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GROOVER & HOLMES			PARRIES, DRU M	
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/657,053	BOECKMANN, EDUARD F.
	Examiner Dru M. Parries	Art Unit 2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 07 July 2007.
- 2a) This action is **FINAL**.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-8 and 10-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) 6 and 7 is/are allowed.
- 6) Claim(s) 1-5, 8, 10-12 and 15-20 is/are rejected.
- 7) Claim(s) 13 and 14 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date: _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date: _____	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____

***Response to Arguments***

1. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Sashida et al. (5,257,180). Sashida teaches connecting a remote load (4) to a power converter (100). He also teaches devising an impedance (405a) for a feedback loop (including 406a) according to a desired relative feedback loop gain (desired gain is the gain required to output a desired voltage command value). He also teaches an additional feedback loop (including 201) that is physically closer to the power converter than the remote load.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 5, 10-12 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sashida et al. (5,257,180). Regarding claims 1 and 5, Sashida teaches a power system with two parallel inverters (11, 21) with their outputs combined to power a single load (4). His power

system teaches a first feedback loop (including 300) being connected and physically adjacent to the power converter, and a second feedback loop (including 406a) in parallel with the first loop, and connected to a remote load (4). The first loop is not being directly connected to a load and having a faster response time than the second loop. He also teaches an error amplifier (403) connected to both of the feedback loops.

Regarding claims 10-12, Sashida also teaches a loop impedance (i.e. gain compensation network, 405a), in the feedback loop, relative to a desired loop gain (the desired gain is the gain required to output a desired voltage command value). The first feedback loop includes current detector (406a) and remote load (4). The second feedback loop includes voltage detector (300) and is directly connected to a summing node (503, 504a) input to the error amplifier (403).

Regarding claims 15-20, Sashida teaches the importance of the output voltage/current to the load in the system (i.e. a converter terminal voltage). He teaches determining and setting an impedance (405a) in a feedback loop based on the output voltage/current values, the desired relative gains of each feedback loop, and a specific feedback loop response (i.e. restricting cross current). Sashida also teaches monitoring the voltage at the critical point (output to load) from a summing node (503, 504a) of an error amplifier (403). He also teaches the impedance being set using a resistor-capacitor network (Col. 10, lines 30-31).

Sashida fails to teach a plurality of loads. It would have been obvious to one of ordinary skill in the art at the time of the invention to add on a duplicate of Sashida's invention (i.e. another pair of inverter devices supplying power to another load) to the first pair of inverter devices and load, since it has been held that a mere duplication of the working parts of a device has no patentable significance unless a new and unexpected result is produced. *In re Harza*, 124 USPQ 378. Modifying the initial Sashida power system by adding a duplicate system on top of

it now gives a plurality of loads, each located in a respective feedback loop, and the power converter consisting of all elements with reference numbers 100, 400-404, 407-409, and 500-505. This modification allows for more loads to be powered by stable AC output voltages.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sashida et al. (5,257,180) as applied to claim 1 above, and further in view of Balakrishnan et al. (2005/0141246). Sashida teaches a power supply device as described above. Sashida fails to teach a feedback path including a low-pass filter or a capacitor-resistor network. Balakrishnan teaches a voltage feedback path including a low-pass filter comprising a capacitor-resistor network ([0029], lines 1-4; Fig. 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate a low-pass filter into the voltage feedback path of Sashida's invention so that it could filter out the voltage spikes.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sashida et al. (5,257,180) as applied to claim 1 above, and further in view of Komatsuzaki (JP 06-038537). Sashida teaches a power supply device as described above. Sashida fails to teach a feedback path including a high-pass filter. Komatsuzaki teaches a voltage feedback path including a high-pass filter (Constitution). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate a high-pass filter into the voltage feedback path of Sashida's invention so that it could filter out signals that are too low and could be misinterpreted.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sashida et al. (5,257,180) as applied to claim 1 above, and further in view of De Groot (6,465,992). Sashida teaches a power supply device as described above. Sashida fails to teach a feedback path including a band-pass filter. De Groot teaches a voltage feedback path including a band-pass filter (Abstract). It would have been obvious to one of ordinary skill in the art at the time of the

invention to incorporate a band-pass filter into the voltage feedback path of Sashida's invention so that it will reduce the ripple voltage around the passband.

*Allowable Subject Matter*

6. Claims 6 and 7 are allowed.
7. Claims 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: the references of record, either alone, or in combination, do not teach or suggest at least the limitations of: Regarding claim 13, the specific equation of the output of the error amplifier, and claim 14, for the same reasons as claim 6.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

*Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dru M. Parries whose telephone number is (571) 272-8542. The examiner can normally be reached on Monday -Thursday from 9:00am to 6:00pm. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry, can be reached on 571-272-2800 x 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMP

9-11-2007



MICHAEL SHERRY  
SUPERVISORY PATENT EXAMINER